UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/089,424	07/16/2002	Dieter Foedlmeier	1406/53	7014

25297 7590 03/21/2005

JENKINS, WILSON & TAYLOR, P. A.
3100 TOWER BLVD
SUITE 1400
DURHAM, NC 27707

EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/089,424	FOEDLMEIER, DIETER	
	Examiner	Art Unit	
	Paul B Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/28/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: It appears that the term "PCT" line 1 of claim 1 is a typographical error. For examination purposes, examiner assumes that "PCT" was intended to be "PCI." Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Moran, US Patent no. 6,091,617.

Regarding claim 1, Moran discloses a PCI bus interface circuit for the voltage supply of a PCI plug-in card that can be connected to a PCI bus, having:

a first input [Vcc in Figure 2] for connection to a main voltage supply line of the PCI bus [column 2, lines 36-41];

a second input [Vaux in Figure 2] for connection to an auxiliary voltage supply line of the PCI bus [column 2, lines 36-41];

an output for outputting a supply voltage to the PCI plug-in card [MAIN POWER SUPPLY FOR ADAPTER in Figure 2];

a first switching device [Q3 in Figure 2] for switching a main supply voltage that is present at the first input to the output if no auxiliary supply voltage V_{aux} is present at the second input [column 2, lines 50-55];

a second switching device [Q2 in Figure 2] for switching an auxiliary supply voltage V_{aux} that is present at the second input to the output if no main supply voltage V_{cc} is present at the first input [column 2, lines 43-49]; and

a third switching device [Q1 in Figure 2], which, given the simultaneous presence of a main supply voltage V_{cc} at the first input and an auxiliary supply voltage V_{aux} at the second input, drives the second switching device for switching the auxiliary supply voltage V_{aux} through to the output [column 2, lines 43-49 and 62-67].

Regarding claims 2 and 3, Moran further discloses that the switching devices are transistors with each having control terminals [Figure 2].

Regarding claim 4, Moran further discloses that the switching devices are transistors, the third switching device being constructed complementarily with respect to the first and second switching devices [Figure 2].

Regarding claim 5, Moran further discloses that the control terminal of the first transistor is connected to the second input and the control terminal of the second transistor is connected to the first input [Figure 2].

Regarding claim 6, Moran further discloses that the control terminal of the third transistor is connected to the second input, the third transistor, when an auxiliary supply voltage is applied to the second input, turning on and connecting the control terminal of the second transistor to a

specific voltage potential, with the results that the auxiliary supply voltage is switched through to the output [Figure 2 and column 2, lines 43-49 and 62-67].

Regarding claim 7, Moran further discloses that respective current limiting resistors are connected upstream of the control terminals of the first and second transistors [Figure 2].

Regarding claim 12, Moran discloses that Vaux is approximately 3.3 volts and that Vcc is approximately 5.0 volts, but a voltage regulator may be included to regulate the vaoltage level of Vcc [column 2, lines 40-43 and 55-57].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moran, US Patent no. 6,091,617.

Regarding claim 8, Moran does not explicitly disclose using a voltage divider to adjust the switching point of the third transistor. However, voltage dividing circuitry is well known in the art. It would have been obvious to one of ordinary skill in the art to use well known voltage dividing circuitry to make the PCI bus interface circuit more flexible by adjusting the switching point of the third transistor.

Regarding claim 9, Moran does not explicitly disclose voltage detection circuitry for detecting the voltage level of the auxiliary voltage supply. However, voltage level detection

circuitry is well known in the art. It would have been obvious to one of ordinary skill in the art include voltage level detection circuitry in the PCI bus interface circuit to ensure that the auxiliary voltage level is within the proper range.

Regarding claims 10 and 11, Moran does not explicitly disclose using transistors with less than a 0.1 volt voltage drop in the turned-on state. However, transistors with less than .1 volt voltage drops are well known in the art and it would have been obvious to one of ordinary skill in the art to use the well known low voltage drop transistors in the PCI bus interface circuit to reduce unnecessary voltage loss of the voltages supplied to the PCI card.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dorsey et al., US Patent no. 6,008,550, discloses using a FET with a voltage drop of less than 50mV.

Ho et al., US Patent no. 6,560,714, discloses a method of selecting a voltage to be supplied to a PCI device.

Ho et al., US Patent no. 6,564,333, discloses a method of selecting a voltage to be supplied to a PCI device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
March 16, 2005